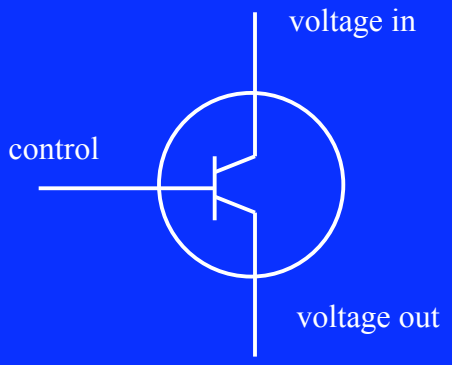
Transistors and Logic Circuits

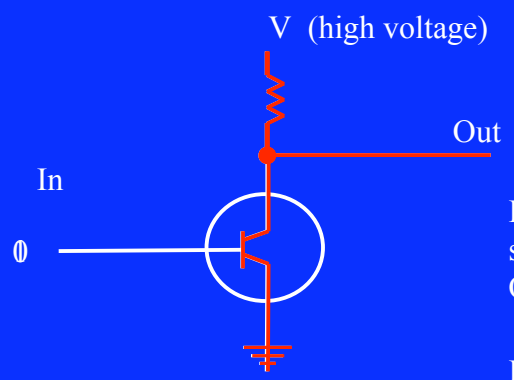
Transistor



control high allows
current to flow --
switch is closed (on)

control low stops
current flow
switch is open (off)

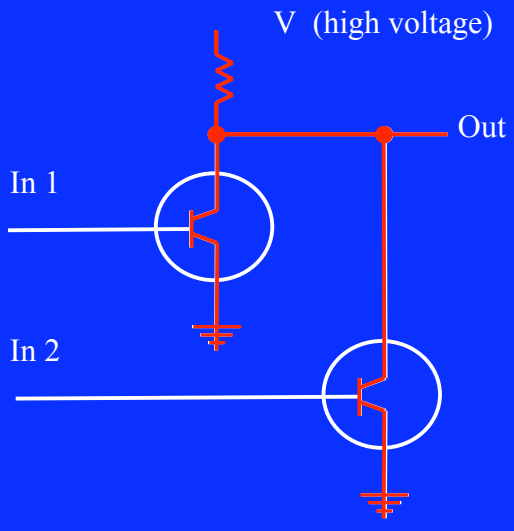
NOT Gate One transistor



In = high, switch is closed so current flows to ground Out is low.

In = low, switch is open so current flows to Out Out is high.

NOR Gate Two transistors

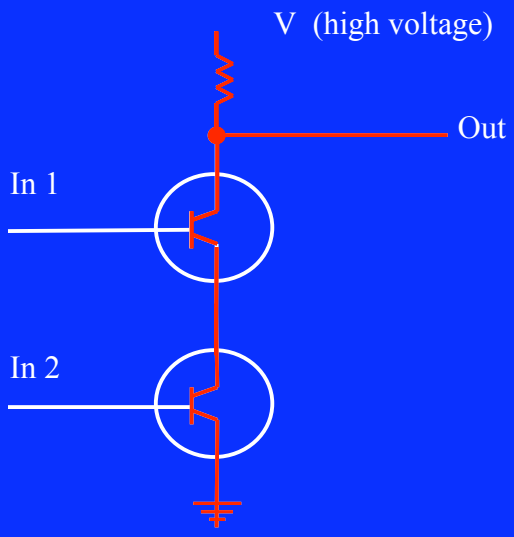


In 1 = 1, Out = 0

In 2 = 1, Out = 0

In 1 = 0
In 2 = 0, Out = 1

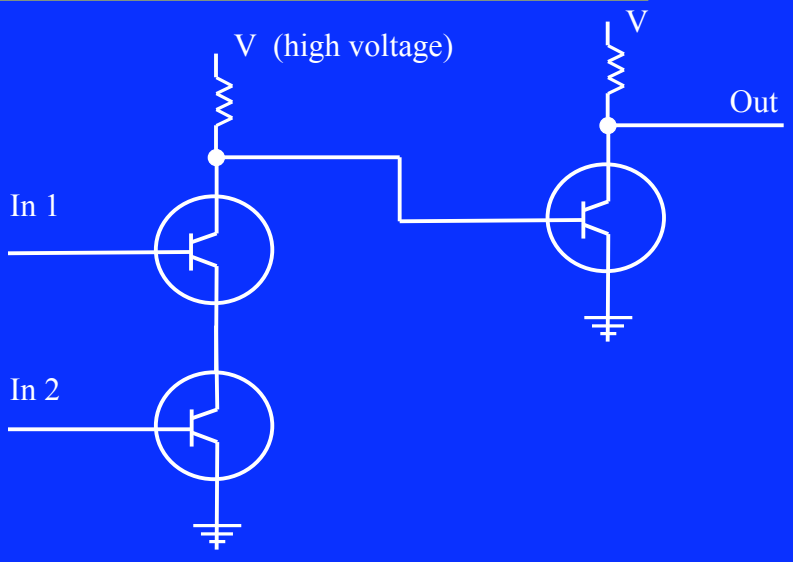
NAND Gate Two transistors



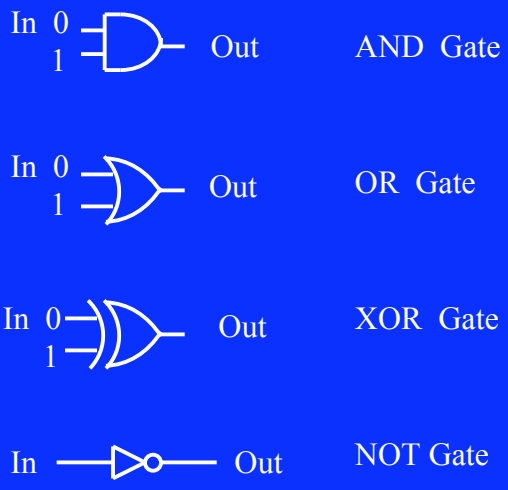
In 1 = 1,
In 2 = 1, Out = 0

In 1 = 1
In 2 = 0, Out = 1

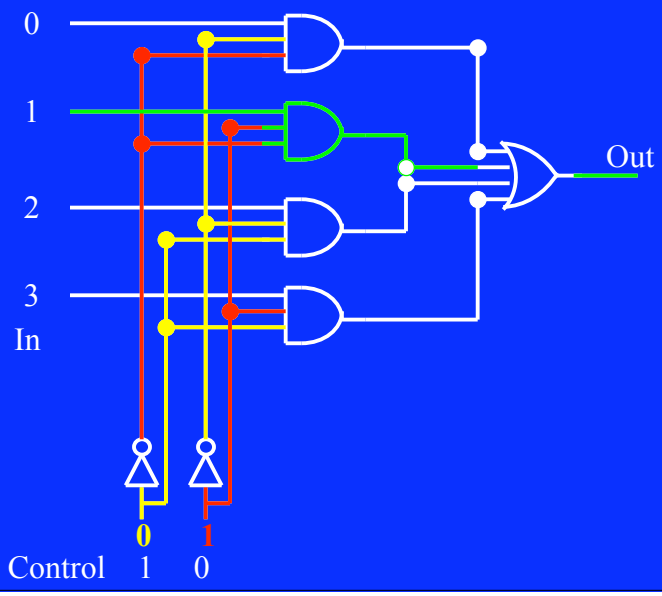
AND Gate Three transistors



Logic Gates

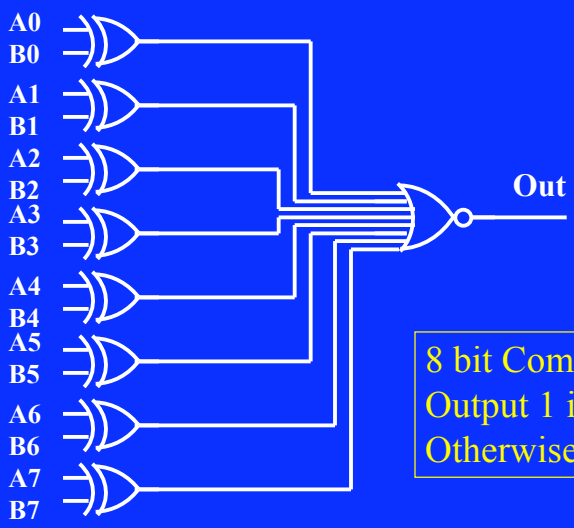


Logic Circuit -- 4 input Multiplexor



Logic Circuit Puzzle 1

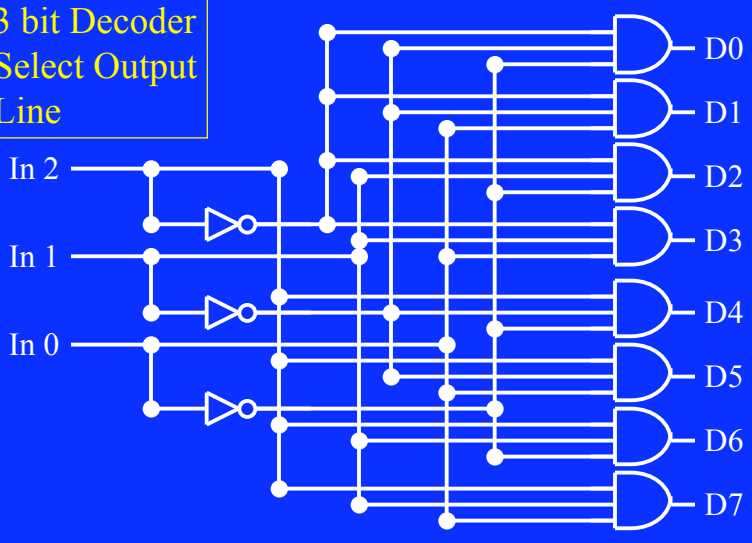
Input Binary Numbers A, B



8 bit Comparator
Output 1 if A = B
Otherwise 0

Logic Circuit Puzzle 2

3 bit Decoder
Select Output Line



Programmable Logic Array

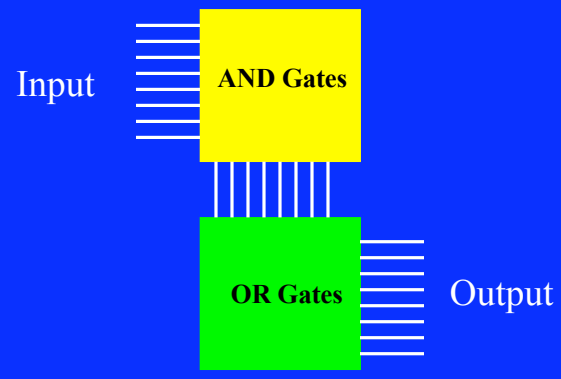
- Any Logic Truth Table can be implemented
- Uses block of AND gates followed by block of OR gates
- Programmable
  - once
  - many times
- Used for implementing different circuits

Truth Table to Normal Form

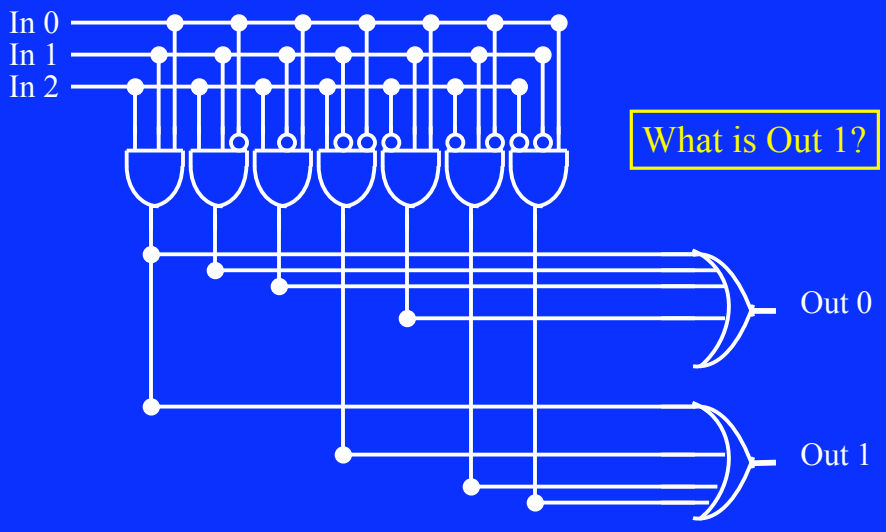
A	B	C	expression	
1	1	1	1	A and B and C
1	1	0	1	A and B and ~C
1	0	1	1	A and ~B and C
1	0	0	0	
0	1	1	1	~A and B and C
0	1	0	0	
0	0	1	0	
0	0	0	0	

(A and B and C) or (A and B and ~C)
or (A and ~B and C) or (~A and B and C)

PLA


Input
AND Gates
OR Gates
Output

PLA


In 0
In 1
In 2
What is Out 1?
Out 0
Out 1

Normal Form to Truth Table

A	B	C	expression	
1	1	1	1	A and B and C
1	1	0	0	
1	0	1	0	Odd Parity
1	0	0	1	A and ~B and ~C
0	1	1	0	
0	1	0	1	~A and B and ~C
0	0	1	1	~A and ~B and C
0	0	0	0	

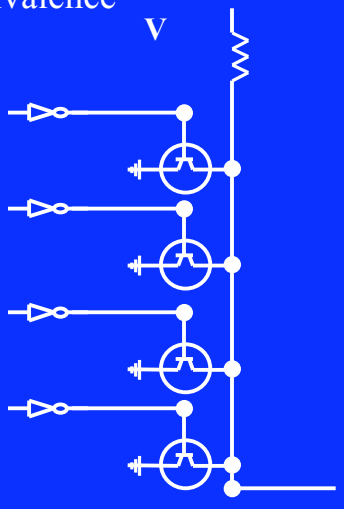
(A and B and C) or (A and ~B and ~C)
or (~A and B and ~C) or (~A and ~B and C)

PLA, Alternate Representation

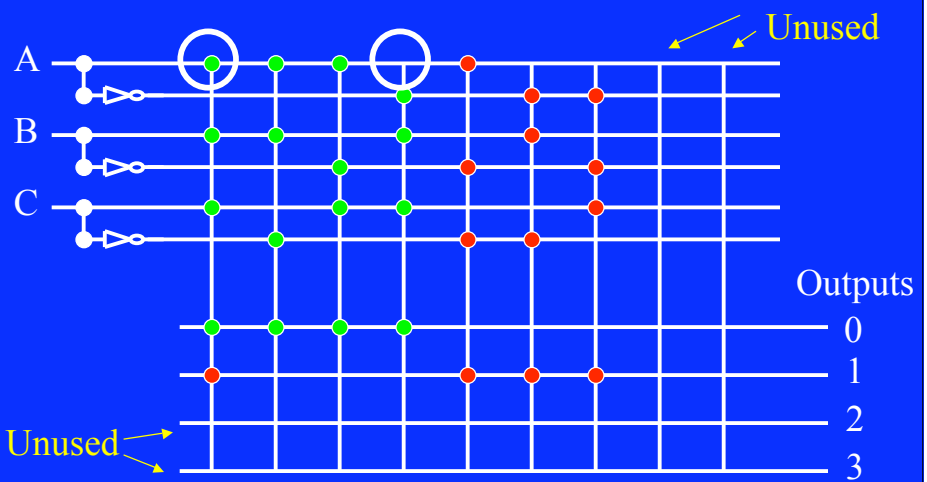
AND Block uses DeMorgan Equivalence

A and B = not (not A or not B)

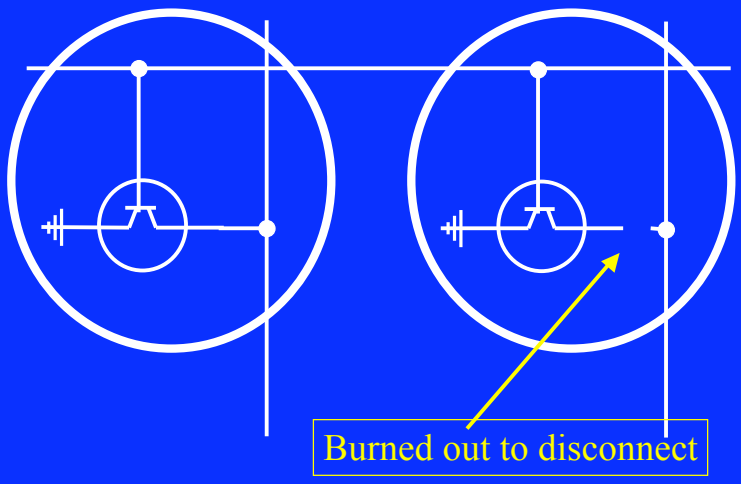
OR Block uses direct or



PLA, Alternate Representation



PLA, Alternate Representation



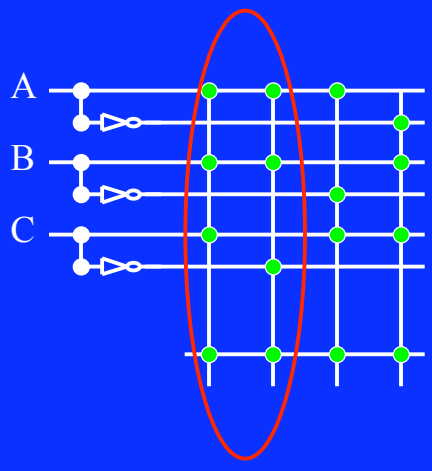
PLA "Don't Cares"

A	B	C	exp
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

A	B	C	exp
1	1	X	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

X = Don't Care

PLA "Don't Cares"



Reduce number of PLA lines used for expression