Specifications for the TB Inc. machine:

Memory: 1K

word: 24 bits

Registers: A, X, PC, MAR, MDR, IR, CC.
A: accumulator
X: used for comparison to set CC
PC: program counter
MAR: memory address register
MDR: memory data register
IR: instruction register
CC = 0 when equal, 1 when <, and 2 when >.

Hardware Stack: must accommodate up to 10 entries

Instruction Set:

Mneumonic	Opcode in hex	Effect
ADD m	40	A ← (A) + mword
STA m	0C	mword ← (A)
STCH m	54	m ← rightmost byte (A)
STX m	10	mword ← (X)
J m	3C	PC ← mword
JSUB m	48	Push(PC, thestack); PC ← mword
RSUB	4C	Pop(PC, thestack)
LDA m	00	A ← mword
LDCH m	50	A (rightmost byte) ← m
HALT	FF	halt the CPU
LDX m	04	X ← mword
COMP m	28	Set CC by (A):(mword)
TIX m	2C	X ← (X + 1); CC set by (X):mword

mword: memory word
A means the register itself.
(A) means the contents of A.

Addressing modes indicated by bits 8, 9, and 10:

000	direct	
010	indexed	based on the X register
001	indirect	
011	indexed indirect	
1	immediate	

Opcode form:

bits 0 - 7	opcode given in hexadecimal
bit 8	immediate mode indicator
bit 9	indexed addressing bit if bit 8 = 0
bit 10	indirect addressing bit if bit 8 = 0
bits 9 - 23	operand value (if immediate) all values right adjusted; zero fill or truncate as needed

I/O

One way to think of input is as records containing pairs of characters which simulate pairs of hexadecimal digits. Each pair of hex digits comprises a byte. An input record can have multiple contiguous bytes.

Error Detection

Your emulator should recognize incorrect opcodes and addresses beyond the bounds of available memory, in which case the emulator should terminate with an appropriate message. You should consider what other errors can and should be detected and what messages should appear to help the programmer.