- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  - **Fanout to 15 F Devices**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

CD54AC04 . . . F PACKAGE
CD74AC04 . . . E OR M PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y
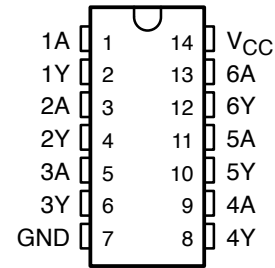
description

The 'AC04 devices contain six independent inverters. The devices perform the Boolean function $Y = \overline{A}$.
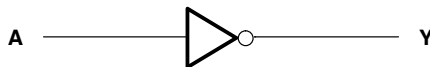
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP – E	Tube	CD74AC04E	CD74AC04E
	SOIC – M	Tube	CD74AC04M	AC04M
		Tape and reel	CD74AC04M96	
	CDIP – F	Tube	CD54AC04F3A	CD54AC04F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)

TEXAS INSTRUMENTS

- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**

- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**

- **Balanced Propagation Delays**

- **Buffered Inputs**

- **±24-mA Output Drive Current**
  - **Fanout to 15 F Devices**

- **SCR-Latchup-Resistant CMOS Process and Circuit Design**

- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

CD54AC08 . . . F PACKAGE
CD74AC08 . . . E OR M PACKAGE
(TOP VIEW)

```
        ___ ___
1A  [ 1      14 ] V_CC
1B  [ 2      13 ] 4B
1Y  [ 3      12 ] 4A
2A  [ 4      11 ] 4Y
2B  [ 5      10 ] 3B
2Y  [ 6       9 ] 3A
GND [ 7       8 ] 3Y
```
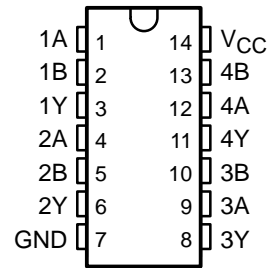
description

The 'AC08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

ORDERING INFORMATION

T$_A$	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP – E	Tube	CD74AC08E	CD74AC08E
	SOIC – M	Tube	CD74AC08M	AC08M
		Tape and reel	CD74AC08M96	
	CDIP – F	Tube	CD54AC08F3A	CD54AC08F3A

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

logic diagram, each gate (positive logic)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**

- **Max t_{pd} of 7.5 ns at 5 V**

SN54AC11 . . . J OR W PACKAGE
SN74AC11 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

1A	1	14 V_{CC}
1B	2	13 1C
2A	3	12 1Y
2B	4	11 3A
2C	5	10 3B
2Y	6	9 3C
GND	7	8 3Y
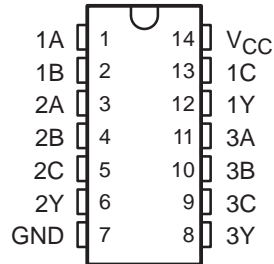
SN54AC11 . . . FK PACKAGE
(TOP VIEW)
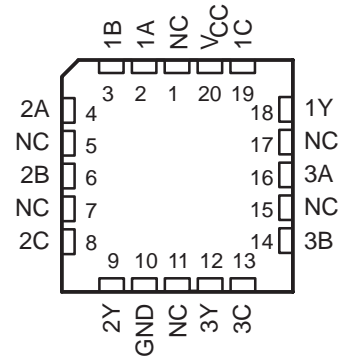
NC – No internal connection

description/ordering information

The 'AC11 devices contain three independent 3-input AND gates. These devices perform the Boolean function $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74AC11N	SN74AC11N
	SOIC – D	Tube	SN74AC11D	AC11
		Tape and reel	SN74AC11DR	
	SOP – NS	Tape and reel	SN74AC11NSR	AC11
	SSOP – DB	Tape and reel	SN74AC11DBR	AC11
	TSSOP – PW	Tube	SN74AC11PW	AC11
		Tape and reel	SN74AC11PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54AC11J	SNJ54AC11J
	CFP – W	Tube	SNJ54AC11W	SNJ54AC11W
	LCCC – FK	Tube	SNJ54AC11FK	SNJ54AC11FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

logic diagram, each gate (positive logic)

```
1A  1
1B  2        ┐
1C  13       ├──D──  12  1Y


2A  3
2B  4        ┐
2C  5        ├──D──  6   2Y


3A  11
3B  10       ┐
3C  9        ├──D──  8   3Y
```

Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀DB package .... 96°C/W
⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀N package .... 80°C/W
⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀NS package .... 76°C/W
⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀PW package .... 113°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
⠀⠀⠀⠀⠀⠀2. The package thermal impedance is calculated in accordance with JESD 51-7.

- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply**
- **Buffered Inputs**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  - **Fanout to 15 F Devices**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

CD54AC32 . . . F PACKAGE
CD74AC32 . . . E OR M PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y
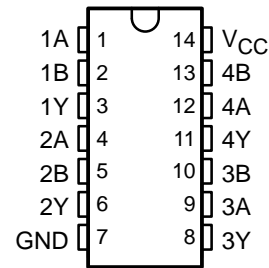
description/ordering information

The 'AC32 devices are quadruple 2-input positive-OR gates. These devices perform the Boolean function $Y = \overline{\overline{A} \bullet \overline{B}}$ or $Y = A + B$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP – E	Tube	CD74AC32E	CD74AC32E
	SOIC – M	Tube	CD74AC32M	AC32M
		Tape and reel	CD74AC32M96	
	CDIP – F	Tube	CD54AC32F3A	CD54AC32F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	X	H
X	H	H
L	L	L

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package .... 80°C/W
                             M package .... 86°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
          2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			$T_A = 25°C$		$-55°C$ to $125°C$		$-40°C$ to $85°C$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 1.5$ V	1.2		1.2		1.2		V
		$V_{CC} = 3$ V	2.1		2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 1.5$ V		0.3		0.3		0.3	V
		$V_{CC} = 3$ V		0.9		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 4.5$ V to 5.5 V		−24		−24		−24	mA
I_{OL}	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.5$ V to 3 V		50		50		50	ns/V
		$V_{CC} = 3.6$ V to 5.5 V		20		20		20	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
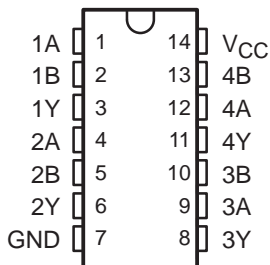
- **4.5-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**

- **Max t_{pd} of 10 ns at 5 V**
- **Inputs Are TTL-Voltage Compatible**

SN54ACT86 . . . J OR W PACKAGE
SN74ACT86 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

SN54ACT86 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1B (3), 1A (2), NC (1), V_{CC} (20), 4B (19)

1Y	4	18	4A
NC	5	17	NC
2A	6	16	4Y
NC	7	15	NC
2B	8	14	3B

Bottom pins: 2Y (9), GND (10), NC (11), 3Y (12), 3A (13)
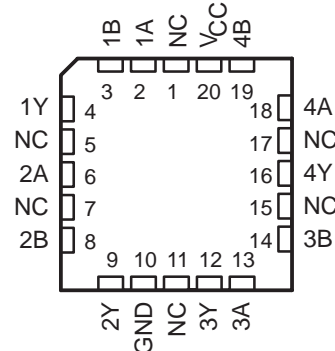
NC – No internal connection

description/ordering information

The 'ACT86 devices are quadruple 2-input exclusive-OR gates. The devices perform the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74ACT86N	SN74ACT86N
	SOIC – D	Tube	SN74ACT86D	ACT86
		Tape and reel	SN74ACT86DR	
	SOP – NS	Tape and reel	SN74ACT86NSR	ACT86
	SSOP – DB	Tape and reel	SN74ACT86DBR	AD86
	TSSOP – PW	Tube	SN74ACT86PW	AD86
		Tape and reel	SN74ACT86PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54ACT86J	SNJ54ACT86J
	CFP – W	Tube	SNJ54ACT86W	SNJ54ACT86W
	LCCC – FK	Tube	SNJ54ACT86FK	SNJ54ACT86FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

FUNCTION TABLE
(each gate)

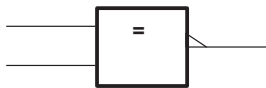| INPUTS		OUTPUT
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.
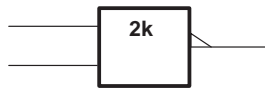
EXCLUSIVE-OR
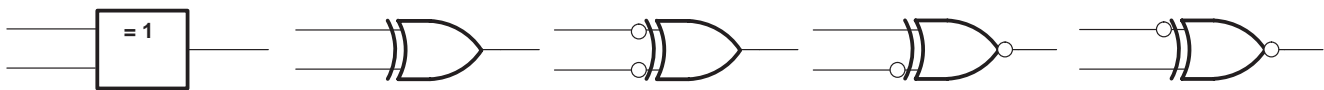
These five equivalent exclusive-OR symbols are valid for an 'ACT86 gate in positive logic; negation may be shown at any two ports.
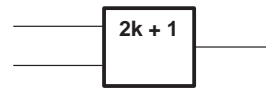
LOGIC-IDENTITY ELEMENT	**EVEN-PARITY ELEMENT**	**ODD-PARITY ELEMENT**
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).	The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.	The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
                       DB package .... 96°C/W
                       N package .... 80°C/W
                       NS package .... 76°C/W
                       PW package .... 113°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The package thermal impedance is calculated in accordance with JESD 51-7.